IN THE CLAIMS:

Please amend claims 2, 9-11, 17, 19, and 21 into the following form:

2. (Amended) A current mirror circuit comprising:

a current source;

a first MOS transistor having a gate, a drain coupled to the gate and the current source, and a source coupled to a first power source;

a second MOS transistor having a gate coupled to the gate of the first MOS transistor, a drain coupled to a second power source, and a source coupled to the first power source, the second MOS transistor being the same channel type as the first MOS transistor, a mirror current flowing into the drain of the second MOS transistor, the mirror current corresponding to the current source; and

a compensation circuit coupled to the drain of the first MOS transistor and the second MOS transistor, the compensation circuit configured to decrease the mirror current against an increase of absolute value of a drain voltage of the second MOS transistor.

9. (Amended) A current mirror circuit comprising:

a current source;

a first PMOS transistor having a gate, a drain coupled to the gate and the current source, and a source coupled to a first power source, the gate of the first PMOS transistor applied a voltage V_{g1};

a second PMOS transistor having a gate coupled to the gate of the first PMOS transistor, a drain coupled to a second power source, and a source coupled to the first power source, a

mirror current flowing into the drain of the second PMOS transistor, the mirror current corresponding to the current source; and

a compensation circuit comprising:

at least one compensation PMOS transistor, each compensation PMOS transistor having a gate, a source coupled to the first power source, and a drain coupled to the drain of the second PMOS transistor; and

at least one subtracter coupled to the drain of the first PMOS transistor and the second PMOS transistor, each subtracter configured to supply a voltage which is higher than the voltage V_{gl} to the gate-source of each compensation PMOS transistor.

10. (Amended) The current mirror circuit according to claim 9, wherein

the compensation PMOS transistor has a gate length and a channel width, respectively, equal to those of the second PMOS transistor.

11. (Amended) The current mirror circuit according to claim 9, wherein

each of the subtracters supplies a voltage expressed by an arithmetic series a_k to the gate-source of the at least one compensation PMOS transistor respectively, where a_k is the arithmetic series equal to:

$V_{gl} - kV_{dl}$ $(k = 1, 2, \ldots, n)$, wherein

V_{dl} is the drain-source voltage of the second transistor,

V_{gl} is the gate-source voltage of the second transistor, and

n is the number of PMOS transistors of the compensation circuit.

17. (Amended) A current mirror circuit comprising:

a current source;

a first group of at least two PMOS transistors connected in series, wherein each of the first group of PMOS transistors has a gate, a drain coupled to the gate, and a source, wherein the source of a first PMOS transistor of the first group of PMOS transistors is coupled to a first power source, wherein the first PMOS transistor of the first group of PMOS transistors is defined as being electrically closest to the first power source;

a second group of PMOS transistors connected in series, wherein the number of PMOS transistors in the second group of PMOS transistors is equal to the number of PMOS transistors in the first group of PMOS transistors, each PMOS transistor of the second group having a gate coupled to the gate of a corresponding PMOS transistor of the first group, a drain, and a source, wherein the source of a first PMOS transistor of the second group of PMOS transistors is coupled to the first power source, wherein the first PMOS transistor of the second group of PMOS transistors is defined as being electrically closest to the first power source, wherein the drain of a last PMOS transistor of the second group of PMOS transistors is coupled to a second power source, wherein the last PMOS transistor of the second group of PMOS transistors is defined as being electrically furthest from the first power source; and

a compensation circuit comprising:

a third group of PMOS transistors connected in series, wherein the number of PMOS transistors in the third group of PMOS transistors is equal to the number of PMOS transistors in the second group of PMOS transistors, each of the third group of PMOS transistors having a gate, a source, and a drain, wherein the source of a first PMOS

transistor of the third group of PMOS transistors is coupled to the first power source, wherein the first PMOS transistor of the third group of PMOS transistors is defined as being electrically closest to the first power source, wherein the drain of a last PMOS transistor of the third group of PMOS transistors is coupled to the second power source, wherein the last PMOS transistor of the third group of PMOS transistors is defined as being electrically furthest from the first power source; and

a group of subtracters, each subtracter coupled to the drain of a corresponding PMOS transistor of the first group, the source of a corresponding PMOS transistor of the second group, and the gate of a corresponding PMOS transistor of the third group, each subtracter configured to supply difference voltages between gate-source voltages and drain-source voltages of the corresponding second group of PMOS transistors to the gate of the third PMOS transistors in the same position in series as the second group of PMOS transistors respectively.

19. (Amended) A power source circuit comprising:

a first PMOS transistor having a source coupled to a first power source, a gate, and a drain coupled to a second power source; and

a compensation circuit comprising:

more than one compensation PMOS transistor, each compensation PMOS transistor having a gate, a source coupled to the first power source, and a drain coupled to the second power source and the drain of the first PMOS transistor; and

more than one subtracter, each subtracter coupled to the gate of a corresponding compensation PMOS transistor, each subtracter configured to supply voltage expressed by an arithmetic series a_k to the gate of the corresponding compensation PMOS transistor, where a_k is the arithmetic series equal to:

$V_{g1} - kV_{d1}$ $(k = 1, 2, \ldots, n)$, wherein

V_{d1} is the drain-source voltage of the first transistor,

V_{g1} is the gate-source voltage of the first transistor, and

n is the number of the PMOS transistors of the compensation circuit.

21. (Amended) A power source circuit comprising:

a first PMOS transistor group having at least two PMOS transistors connected in series, wherein a source of a first PMOS transistor of the first PMOS transistor group is coupled to a first power source, wherein the first PMOS transistor is defined as being electrically closest to the first power source, wherein a drain of a last PMOS transistor of the first PMOS transistor group is coupled to a second power source, wherein the last PMOS transistor is defined as being electrically furthest from the first power source; and

a compensation circuit comprising:

a second PMOS transistor group having at least two PMOS transistors connected in series, wherein a source of a first PMOS transistor of the second PMOS transistor group is coupled to the first power source, wherein the first PMOS transistor is defined as being electrically closest to the first power source, wherein a drain of the last PMOS transistor of the second PMOS transistor group is coupled to the second power source,

wherein the last PMOS transistor is defined as being electrically furthest from the first power source; and

a group of subtracters, each subtracter coupled to a gate of a corresponding PMOS transistor of the second PMOS transistor group, each subtracter configured to supply difference voltages between gate-source voltages and drain-source voltages of the corresponding first group of PMOS transistors to the gate source of the second PMOS transistor which is in the same position in series as the first group of PMOS transistors.

The claim changes made in this Amendment are illustrated in detail in the attached "marked-up" copy of the claims.

Please add the following new claim:

--22. (New) A current mirror circuit comprising:

a current source;

a first MOS transistor having a gate, a drain coupled to the gate, and a source coupled to a first power source;

a second MOS transistor having a gate coupled to the gate of the first MOS transistor, a drain coupled to a second power source, and a source coupled to the first power source, the second MOS transistor having the same channel type as the first MOS transistor, a mirror current flowing into the drain of the second MOS transistor, the mirror current corresponding to the current source; and